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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/328,800	06/09/1999	HIROSHI ITO	H-782	7315

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EXAMINER
FERRIS III, FRED O

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 04/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/328,800	Applicant(s) ITO ET AL.	
	Examiner Fred Ferris	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received:

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-23 have been examined. Claims 1-23 have been rejected by the examiner.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), dated 10 June, 1998 which papers have been placed of record in the file.

Claim Interpretation

3. The claimed invention is disclosed to be a logic module used for logic emulation and verification of electronic circuits. The device falls into the broad category known in the art as circuit emulators and in-circuit emulators (ICE). The logic module (a circuit board) contains numerous programmable large scale integrated circuits (LSI's), programmable cross-point-switches (allowing programmable connections between LSI's), and connectors for external connection and connection to an enhanced logic emulation board. A structure using popular industry techniques for multiple module staging (stacking/platform) and cooling of IC's in the structure is also described.

Claim Objections

*4. Claim 19 objected to because of the following informalities: Claim 19 references an "**integrated circuit fabricating method**" but the claimed invention is not disclosed to be a method for the fabrication of integrated circuits. Appropriate correction is required.*

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 16, 19 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Matter critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See In re Mayhew, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). Specifically, claim 16 references "a logic module supporting programmable logic elements in which said ***integrated circuit*** *is* ***programmed****" but does not specifically provide a method, algorithm, technique, nor describe the hardware/software required to actually* ***program*** *an* ***integrated circuit****. Claim 19 references an* ***integrated circuit fabricating method*** *comprising: "****writing logic data*** *to programmable logic elements,* ***verifying logic data****, and* ***generating circuits****" but does not specifically provide the methods, algorithms, techniques, nor describe the hardware/software required to actually* ***write logic data****,* ***verify logic data****, or* ***generate circuits****. Further, the specification describes a logic module device for logic emulation and verification and does not disclose a method for fabricating integrated circuits.*

Claim Rejections - 35 USC § 102

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent 5,640,337 issued to Huang et al.

Claims 1-9 are drawn to a ***logic emulation module*** *comprising:*

- ***programmable LSIs*** *capable of* ***programming logic***
- ***switching LSIs*** *capable of* ***programming connections***
- ***connectors*** *for* ***external electrical connection***
- *a* ***board*** *on which to* ***mount programmable LSI's***
- ***programmable LSI's*** *and* ***connectors coupled*** *by way* ***switching LSI's***

Per claim 1-9: Huang discloses a ***programmable logic emulation module*** *constructed of a* ***circuit board*** *having* ***through holes*** *and* ***programmable logic devices*** *(LSI's) connected via field* ***programmable interconnect*** *(cross-point-****switches****) containing* ***connectors*** *for* ***external connection*** *used for* ***logic emulation*** *and* ***verification****. (Fig. 2, 3, 5, CL8-L53-62, CL6-L66, CL10-L25-34, CL12-L1, CL13-L25, 44, 55)*

Claims 10 and 11 are drawn to a ***logic mulation board*** *comprising:*

- *connectors for connection to logic emulation* ***(additional) "stacked" module***

- ***terminal lands (pads for mounting)*** *for* ***insertion of LSI chips***.

Per claim 10-11: Huang discloses ***a logic emulation board*** *that includes an* ***additional module (a "pod")*** *which can be incorporated as part of the basic* ***core-cell (module)*** *forming an equivalent pair of* ***"stacked"*** *emulation modules. The Huang device includes* ***sockets*** *for* ***insertion of LSI chips***. *(CL10-L11-45, Fig. 2, 3, 5)*

Claim 12 is drawn to a ***logic emulation device*** *consisting of a* ***logic emulation board*** *connected to a* ***logic emulation (stacked) module*** *including:*

- ***programmable LSIs*** *capable of* ***programming logic***
- ***switching LSIs*** *capable of* ***programming connections***
- ***connectors*** *for* ***external electrical connection***
- *a* ***board*** *on which to* ***mount programmable LSI's***
- ***programmable LSI's*** *and* ***connectors coupled*** *by way* ***switching LSI's***
- ***terminal lands (pads for mounting)*** *for* ***insertions of LSI chips***

Per claim 12: Huang discloses a ***programmable logic emulation module*** *constructed of a* ***circuit board*** *having* ***through holes*** *and* ***programmable logic devices*** *(LSI's) connected via field* ***programmable interconnect*** *(cross-point-****switches****) containing* ***connectors*** *for* ***external connection*** *used for* ***logic emulation*** *and* ***verification***. *Huang also discloses a logic emulation board that includes an additional module (a "pod") which can be incorporated as part of the basic core-cell (module) forming a pair of* ***"stacked"*** *modules.* ***The Huang devic includes*** *sockets*

for insertion of LSI chips. (CL10-L11-45, Fig. 2, 3, 5) Further, the Huang device includes sockets for ***insertion (and mounting)*** *of* ***additional LSI chips.*** *(Fig. 2, 3, 5, CL8-L53-62, CL6-L66, CL10-L25-34, CL12-L1, CL13-L25, 44, 55, CL10-L11-45)*

Claims 13-15 are drawn to logic module (printed circuit) board consisting of:

- ***programmable logic*** *elements (with logic* ***data*** *for logic* ***verification****)*
- ***connectors*** *for exchanging* ***input/output*** *signals*
- ***switching elements*** *for* ***controlling connections*** *between logic elements*

Per claim 13-15: Huang discloses a programmable logic emulation module constructed of a circuit ***board*** *consisting of* ***programmable logic*** *elements with logic* ***data*** *for logic* ***verification,*** *connectors for exchanging input/output signals, and* ***switching elements*** *for* ***controlling connections*** *between logic elements. (Fig. 2, 3, 5, CL8-L53-62, CL6-L66, CL10-L25-34, CL12-L1, CL13-L25, 44, 55, CL10-L11-45)*

Claim 16 is drawn to a logic board with integrated circuits including:

- ***terminal lands*** *for connecting IC's*
- ***connectors*** *for a logic module for* ***programming*** *IC's*

Per claim 16: ***Terminal lands*** *for connecting IC's and* ***connectors*** *for external connection are inherent features of nearly all logic (printed circuit) boards as well as referenced prior art. (Huang, Fig 2, 5) Further, Huang supports both on and off board* ***programming*** *of IC logic devices. (Abstract-L13)*

*Claim 17 & 18 are drawn to a **logic verification system** including a logic module implementing IC logic and a logic board carrying IC's (for undergoing logic verification) and including the features of:*

- ***programmable logic** elements (with logic **data** for logic **verification**)*
- ***connectors** for exchanging **input/output** signals*
- ***switching elements** for **controlling connections** between logic elements*
- ***terminal lands** for connecting IC's*
- ***connectors** for a logic module for programming IC's*
- ***programmed logic data** for logic verification*

*Per claim 17, 18: Huang teaches a system (including a logic "pod" module and logic board carrying IC's (undergoing logic verification)) for **logic verification** that includes all of the above listed limitations as previously discussed. Further, Huang provides a means for IC programming (on/off board) and "plug" simulation for early verification. (CL9-L65, CL-11-L23)*

*Regarding claim 19: While claim 19 is deficient and rejected under 35 U.S.C. 112(1) as previously described, the examiner makes 35 U.S.C. 102(b) rejections based on the following observations: Huang teaches **mounting** of programmable logic elements and logic "pod" module (CL12-L15, CL13-L20) and further **verification** (CL9-L65) of programmable logic IC's.*

Regarding claims 20, 21: The teachings of Huang include the limitations of a ***logic module*** *including* ***programmable LSI's***, ***switching IC's***, *a supporting* ***board***, *a* ***connector*** *for external signals, and* ***multiple wirings*** *between connectors and* ***programmable logic elements*** *as previously discussed. (Fig. 2, 3, 5, CL8-L53-62, CL6-L66, CL10-L25-34, CL12-L1, CL13-L25, 44, 55)*

Claims 22, 23 are rejected under 35 U.S.C. 102(a) as being unpatentable over U.S. Patent 6,128,194 issued to Francis.

Claims 22, 23 are drawn to a multiple chip circuit module (board) including:

- ***radiation plate (heat sink)*** *over IC's*
- ***metal spacers***
- ***heat conduction*** *between IC's* ***radiation plate***

Per claim 22, 23: Francis teaches circuit board containing multiple IC's where the IC's are covered (top and bottom) by a heat sink (radiation plate) which is further connected to a bottom cover (heat sink) and separated by metal spacers. The IC's are mounted on heat conducting circuit board material. (Fig. 2-7, Abstract, Summary of Invention, CL2-L11, CL2-L63, CL4-L47-57, CL6-L4-20)

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,006,022 issued to Rhim et al teaches in-circuit emulation and verification.

U.S. Patent 5,331,571 issued to Aronoff et al teaches emulation of integrated circuits.

U.S. Patent 5,339,262 issued to Rostoker et al teaches in-circuit testing and verification.

U.S. Patent 5,462,442 issued to Umemura et al teaches stacked printed circuit boards.

U.S. Patent 5,575,686 issued to Noschese teaches stacked printed circuit boards.

U.S. Patent 5,574,338 issued to Babier et al teaches programmable interconnection.

U.S. Patent 5,748,875 issued to Tzori teaches logic simulation and emulation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 703-305-9670 and whose normal working hours are 8:30am to 5:00pm Monday to Friday.
Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 703-305-3900.
The Official Fax Numbers are:

After-final	(703) 746-7238
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